DMS LAB Limited

730V BiCDMOS process specification

› Description

- 730V 1.0um BiCDMOS process is DMS Lab Limited BCD smart power technologies.
- Technology allows to integrate a power stage with optimized device performance, protection and a control circuit including driver protection and diagnostic elements
- Typical applications are line power supplies for battery charger adapters, standby power supplies for TV or monitors, auxiliary supplies for motor control, etc. The typical breakdown voltage of the power MOSFET more than 730V.
- The process combines vertical HV Power MOSFET, LV NMOS and HV NMOS transistors with enriched depleted channel on the same silicon chip.
- The 14 layers process is available for 730V breakdown voltage of the MOSFET. This process provides locos insulation, one level poly, and one metal level. With this process an optimized n-channel vertical HV Power MOSFET, HV NMOS with enriched and depleted channel transistors, logic NMOS transistors can be made.

	Wafer
	Epi
1	**Well 1**
2	**Well 2**
3	**Active area**
4	**Guard 1**
5	**Guard 2**
6	**Channel adjust 1**
7	**Channel adjust 2**
8	**Gate**
9	**P base**
10	**P+drain**
11	**N+drain**
12	**Contact**
13	**Metal**
14	**Passivation**

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> Key Features

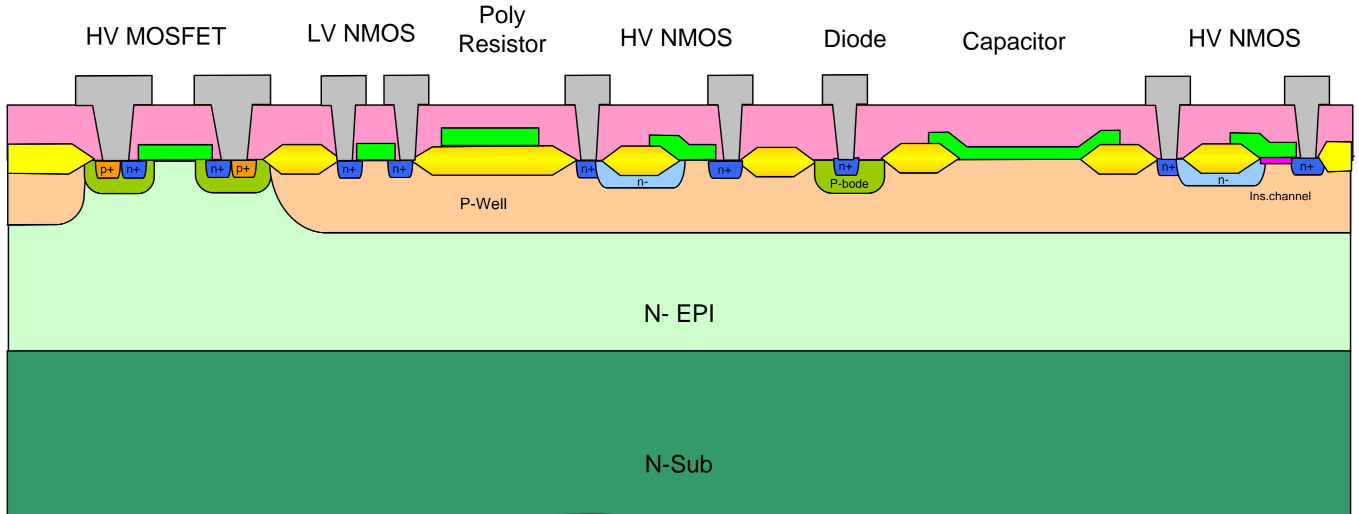
The vertical MOSFET transistor with low Rdson and small area is the main HV component of the BiCDMOS 730V technology.

1.0um one poly, one metal, one PWell BCD process.

A high number of different devices are available:

- 730V n-channel vertical DMOS transistor;
- 10V n-channel MOS transistor;
- 50V enriched and depleted n-channel MOS transistor;
- 50V n-channel MOS transistor;
- 20V Zener diodes;
- Gate oxide capacitors;
- Low resistivity poly-Si resistors;

> Schematic cross section



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> Basic design rules

Layer	Min width (um)	Min spacing (um)
Active Area (CMOS)	2.0	1.5
NMOS Gate	1.5	1.0
Contact	1.0	2.0
Metal-1	4.0	1.5

〉 Device Parameters of main elements for 730V process

ELEMENT	PARAMETER	SPEC		MEASUREMENT CONDITIONS
	UNIT	MIN	MAX	
730V NDMOS L=2.5 um, W=8.5 mm	VTH, V	1.5	2.5	Id=0.1uA
	IDS, A	2.0	-	Ug=Ud=10 V
	BVDS, V	730	-	Id=10uA
	Ron, Ohm	-	17	Ug=10 V
	IDS, uA	-	50	Ug=Ub=Us=0 V, Ud =10 V
HV NMOS L=5 um, W=50 um	VTH, V	0.6	1.0	Id=0.1uA
	IDS, mA	2.0	5.0	Ug=Ud=10 V
	BVDS, V	50	-	Id=10uA
HV NMOS L=5 um, W=50 um insert channel	VTH, V	-2.5	-1.0	Id=0.1uA
	IDS, mA	0.35	-	Ug=Ud=0 V
	BVDS, V	50	-	Id=10uA
LV NMOS L=2.0 um, W=50 um	VTH, V	0.6	1.0	Id=0.1uA
	IDS, mA	7.0	15.0	Ug=Ud=5 V
	BVDS, V	10.0	-	Id=10uA
Zener Diode	BV, V	17.0	23.0	Id=10uA
PolySi-resistor n-type	RS, Ohm/sq	50	70	Ir=10uA
PolySi-resistor p-type	RS, Ohm/sq	110	150	Ir=10uA
PolySi- gate oxide – Well capacitor	Ccs, pF/um2	1,7E-3	2.1E-3	F=1MHz, Vmea=5V